IN THE CLAIMS

1. (Currently amended) An integrated circuit device comprising:

a die having a top surface with a peripheral region and an interior region surrounded by the peripheral region:

a plurality of bond pads disposed in the peripheral region of the die;

at least one internal bus, disposed in the interior region of the die, that distributes power to a plurality of internal node points of the die; and

at least one bond wire connecting at least one of the plurality of bond pads with the at least one internal bus;

wherein the at least one internal bus further comprises at least three separate parallel pairs of internal buses;

a first one of the pairs of internal buses being arranged adjacent and parallel to a first side of the peripheral region;

a second one of the pairs of internal buses being arranged adjacent and parallel to a second side of the peripheral region opposite the first side of the peripheral region; and

a third one of the pairs of internal buses being disposed between and parallel to the first and second pairs.

2. (Original) The integrated circuit device of claim 1, wherein the at least one internal bus comprises a metal power grid.

3. (Original) The integrated circuit device of claim 1, wherein the at least one internal bus comprises at least one internal positive voltage supply bus.

4. (Original) The integrated circuit device of claim 1, wherein the at least one internal bus comprises at least one internal negative voltage supply bus.

5. (Original) The integrated circuit device of claim 1, wherein the at least one internal bus comprises at least one pair of buses comprising an internal positive voltage supply bus and internal negative voltage supply bus.

6. (Original) The integrated circuit device of claim 5, wherein at least one of the voltage supply buses comprises a ground bus.

7. (Original) The integrated circuit device of claim 1, wherein the at least one internal bus comprises bond pads having active circuitry disposed thereunder.

8. (Original) The integrated circuit device of claim 1, wherein at least one of the plurality of bond pads is wire bonded to an integrated circuit package.

9. (Original) The integrated circuit device of claim 1, wherein the at least one of the plurality of bond pads wire bonded to the at least one internal bus is also wire bonded via another bond wire to a positive voltage supply terminal of the device.

10. (Original) The integrated circuit device of claim 9, wherein the positive voltage supply terminal comprises a positive voltage supply ring substantially surrounding the die.

11. (Original) The integrated circuit device of claim 1, wherein the at least one of the plurality of bond pads wire bonded to the at least one internal bus is also wire bonded via another bond wire to a negative voltage supply terminal of the device.

12. (Original) The integrated circuit device of claim 11, wherein the negative voltage supply terminal comprises a negative voltage supply ring substantially surrounding the die.

13. (Original) The integrated circuit device of claim 1, wherein the at least one of the plurality of bond pads wire bonded to the at least one internal bus is connected to another of the plurality of bond pads.

14. (Original) The integrated circuit device of claim 1, further comprising local power interconnects that distribute power from the at least one internal bus to the plurality of internal node points.

15. (Original) The integrated circuit device of claim 1, wherein the plurality of internal node points comprise circuit elements.

16. (Original) The integrated circuit device of claim 1, wherein the power is distributed from the at least one of the plurality of bond pads to at least one secondary bond pad through a metal connector, and from the at least one secondary bond pad to the at least one internal bus through at least one wire bond connection within the peripheral region of the die.

17. (Original) The integrated circuit device of claim 1, wherein the at least one of the plurality of bond pads comprises at least one pair of bond pads comprising a positive voltage supply bond pad and a negative voltage supply bond pad.

18. (Original) The integrated circuit device of claim 17, wherein the at least one pair of bond pads comprises at least about twelve pairs of bond pads substantially evenly spaced apart in the peripheral region of the die.

19. (Canceled)

20. (Currently amended) A method of constructing an integrated circuit device comprising the following steps:

forming an integrated circuit die having at least one peripheral bond pad and at least one internal bus, the internal bus being configured for distributing power to a plurality of internal node points of the integrated circuit device; and

wire bonding the at least one peripheral bond pad to the at least one internal bus;

wherein the at least one internal bus further comprises at least three separate parallel pairs of internal buses;

a first one of the pairs of internal buses being arranged adjacent and parallel to a first side of the die;

a second one of the pairs of internal buses being arranged adjacent and parallel to a second side of the die opposite the first side of the die; and

a third one of the pairs of internal buses being disposed between and parallel to the first and second pairs.

21. (New) A die configured for use in an integrated circuit device, the die having a top surface with a peripheral region and an interior region surrounded by the peripheral region, the die comprising:

a plurality of bond pads disposed in the peripheral region of the die; and

at least one internal bus, disposed in the interior region of the die, that distributes power to a plurality of internal node points of the die;

wherein the plurality of bond pads and the at least one internal bus are connected by at least one bond wire;

wherein the at least one internal bus further comprises at least three separate parallel pairs of internal buses;

a first one of the pairs of internal buses being arranged adjacent and parallel to a first side of the peripheral region;

a second one of the pairs of internal buses being arranged adjacent and parallel to a second side of the peripheral region opposite the first side of the peripheral region; and

a third one of the pairs of internal buses being disposed between and parallel to the first and second pairs.